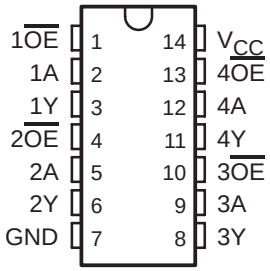
- **Qualified for Automotive Applications**
- **Typical V_{OLP} (Output Ground Bounce) <1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (−16-mA I_{OH}, 32-mA I_{OL})**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

D PACKAGE
(TOP VIEW)



description/ordering information

The SN74ABT125Q-Q1 quadruple bus buffer gate features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION†

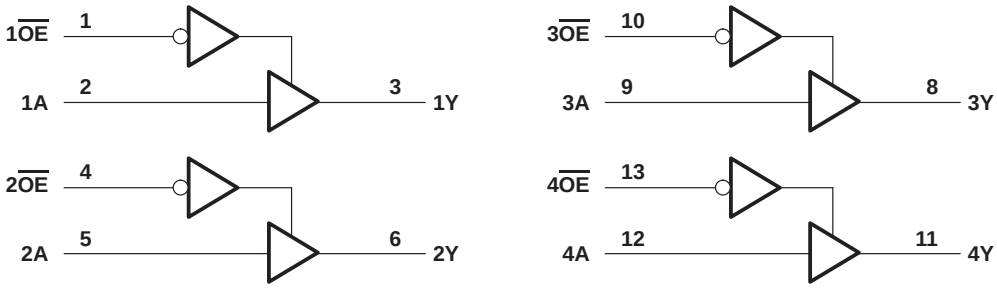
T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	SOIC − D	Tape and reel	SN74ABT125QDRQ1	ABT125Q

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . −0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 126 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . −18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 86°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		−16	mA
I_{OL}	Low-level output current		32	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		µs/V
T_A	Operating free-air temperature	−40	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP†	MAX			
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2		−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.5			2.5		V
		V_{CC} = 5 V,	I_{OH} = −3 mA	3			3		
		V_{CC} = 4.5 V	I_{OH} = −16 mA	2			2		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 32 mA			0.55		0.55	V
V_{hys}					100				mV
I_I		V_{CC} = 0 to 5.5 V,	V_I = V_{CC} or GND			±1		±1	µA
I_{OZPU}		V_{CC} = 0 to 2.1 V, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50		±50	µA
I_{OZPD}		V_{CC} = 2.1 V to 0, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50		±50	µA
I_{OZH}		V_{CC} = 2.1 V to 5.5 V,	V_O = 2.7 V, $\overline{OE}$ ≥ 2 V			10		10	µA
I_{OZL}		V_{CC} = 2.1 V to 5.5 V,	V_O = 0.5 V, $\overline{OE}$ ≥ 2 V			−10		−10	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100			µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50	µA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.5 V	−50	−100	−200§	−50	−200§	mA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250	µA
			Outputs low		24	30		30	mA
			Outputs disabled		0.5	250		250	µA
ΔI_{CC}¶	Data inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5	mA
			Outputs disabled			0.05		0.05	
	Control inputs	V_{CC} = 5.5 V, One input at 3.4 V,	Other inputs at V_{CC} or GND			1.5		1.5	
C_i		V_I = 2.5 V or 0.5 V			3				pF
C_o		V_O = 2.5 V or 0.5 V			7				pF

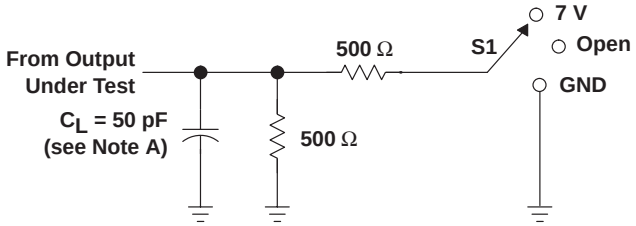
† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This limit may vary among suppliers.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}†	A	Y	1	3.2	4.6	1	6	ns
t_{PHL}†			1	2.5	4.6	1	6.2	
t_{PZH}†	$\overline{OE}$	Y	1	3.6	5	1	6	ns
t_{PZL}†			1	2.5	6.2	1	7.5	
t_{PHZ}	$\overline{OE}$	Y	1	3.8	5.4	1	6.3	ns
t_{PLZ}†			1	3.3	5.3	1	6.5	

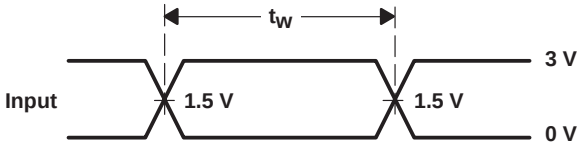
† This limit may vary among suppliers.

PARAMETER MEASUREMENT INFORMATION

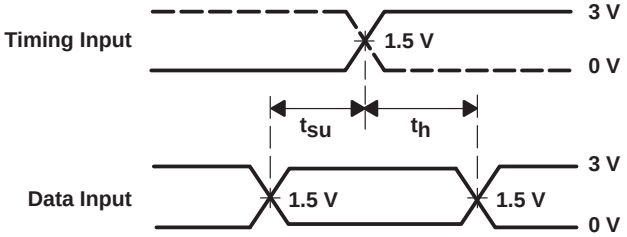


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

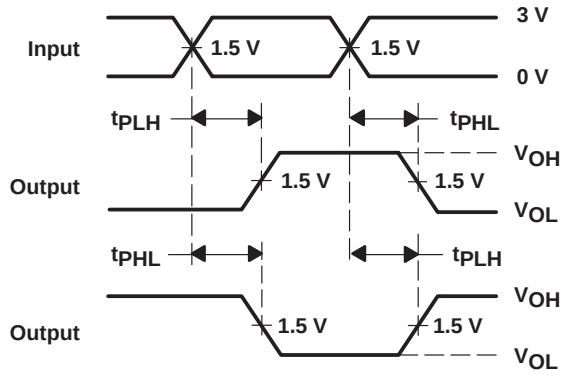
LOAD CIRCUIT



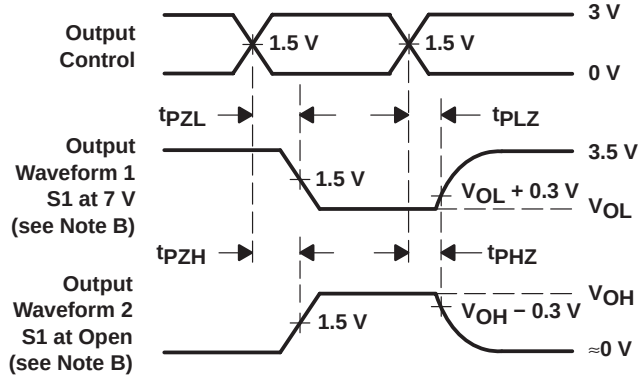
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

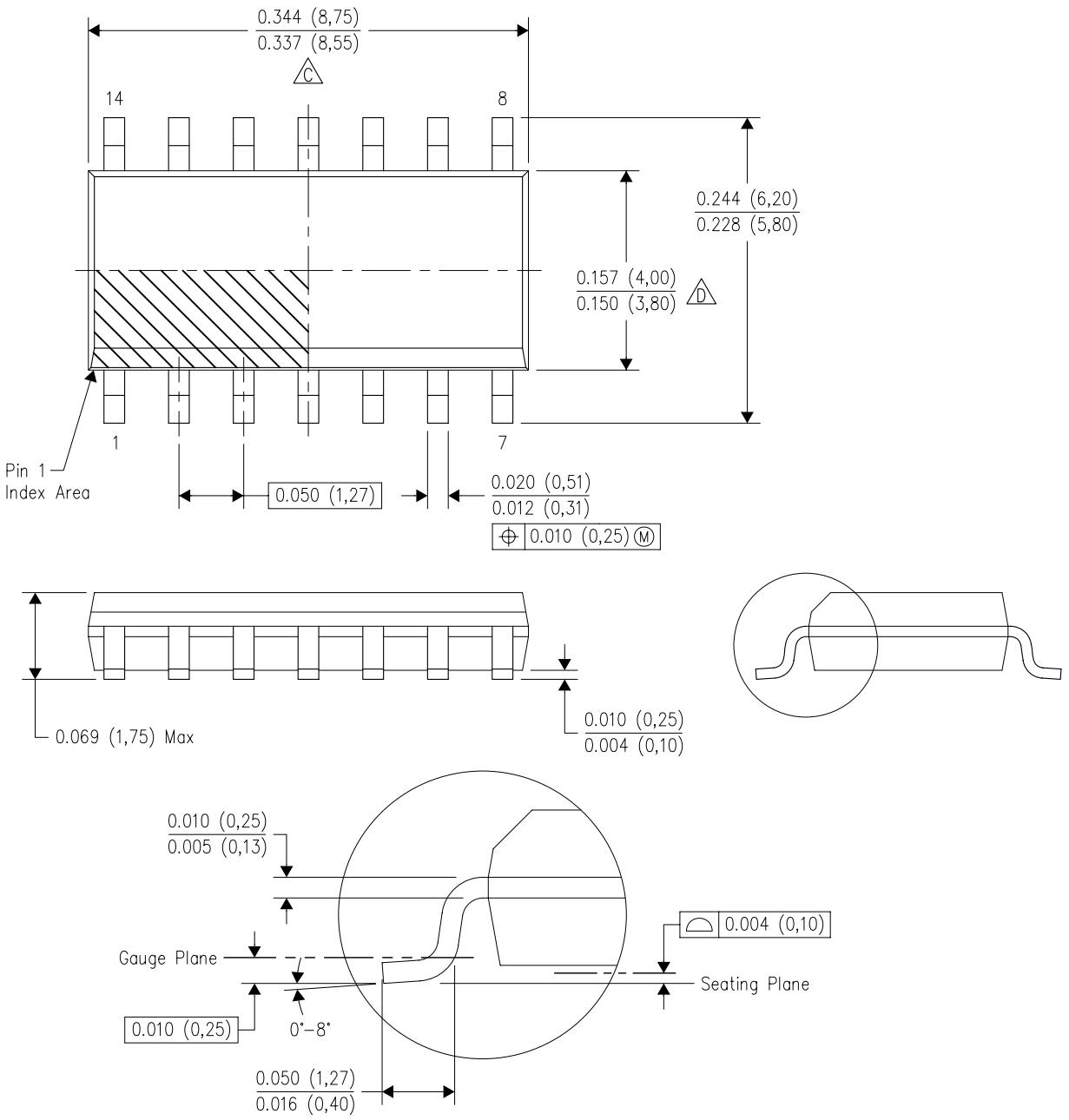
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74ABT125QDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT125QDRQ1	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

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